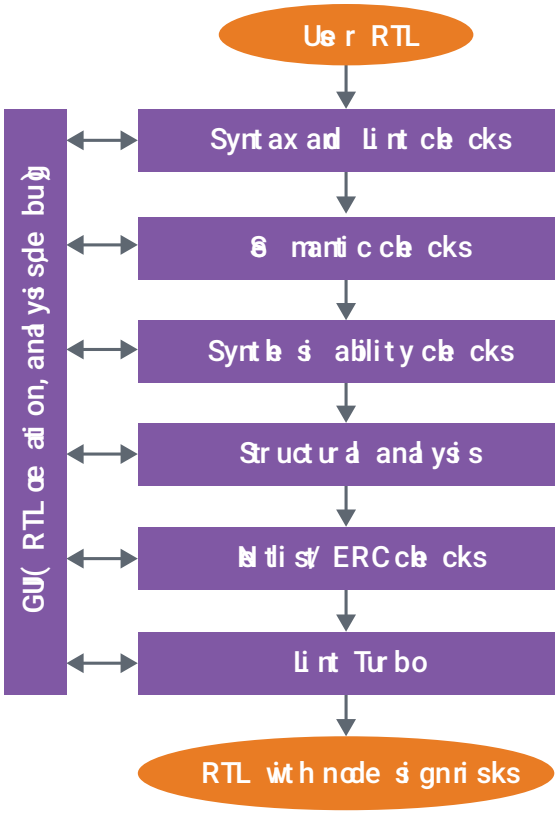
Inefficiencies during RTL design development usually surface as critical design bugs during the late stages of design implementation. If detected late, these bugs often lead to a large number of iterations; if left undetected, they can lead to expensive silicon respins. The VC SpyGlass™ RTL Signoff platform, builds on the proven SpyGlass® technology for early design analysis with the most in-depth analysis at the RTL design phase. VC SpyGlass provides an integrated solution for analysis, debug, and fixing with a comprehensive set of capabilities for structural and electrical issues, all tied to the RTL description of the design.

With increasing complexity and the size of chips, achieving predictable design closure is a challenge. A multitude of coding stu-SEMC -SI

The VC SpyGlass linting solution integrates industry-standard best practices with Synopsys' own extensive experience working with industry-leaders. Lint checks include design reuse compliance checks such as STARC and OpenMORE to enforce a consistent style throughout the design, ease the integration of multi-team and multi-vendor IP, and promote design reuse.



The VC SpyGlass Lint solution dramatically reduces the inherent risk in developing first-pass complex multimillion-gate, nanometer-scale SoCs by accurately detecting design issues at the RTL level. It flags almost all areas of the design that are likely to present implementation challenges.

- Identify critical design issues in RTL with sophisticated static and dynamic analysis
- Integrated comprehensive set of electrical rules check to ensure netlist integrity
- Enables design reuse compliance checks, such as STARC and OpenMORE to enforce a consistent style
- Step-by-step framework to capture and automate customer specific design rules
- Native integration with Verdi® provides a debug environment to enable easy cross-probing between violation reports, schematic and RTL source
- Supports Verilog, VHDL, SystemVerilog and mixed-language designs
- Tcl shell for efficient rule execution and design querying
- SoC abstraction flow for faster performance and low noise

VC SpyGlass Lint provides a structured, easy-to-use, and comprehensive method for solving RTL design issues, thereby ensuring high-quality RTL with fewer but meaningful violations.

- GuideWare™ methodology documentation and rule-sets included
- Infrastructure for rule selection and customization aligned with design milestones
- Guided steps for completing a series of recommended steps to ensure design compliance to HDL standards, coding style, synthesis, simulation, verification, connectivity, clock and reset issues
- Step-by-step approach detects and fixes design bugs in alignment with design milestones, and ensures predictable design closure without any last-minute surprises or a high volume of violations

VC SpyGlass Lint supports “correct-by-construction” design, leading to early design closure and minimizing costly back-end debugging and iterations.

- Directly integrated advanced VC SpyGlass CDC and VC SpyGlass RDC capabiles RDCriles [illegible] fact. [illegible] q 1.1 [illegible] t supports [illegible]