Low power design techniques add new design elements at different stages of the design flow. Architectural design bugs that violate the principles of low power design may exist even at RTL. Isolation cells are typically synthesized automatically. Retention register connections need to be validated after synthesis and again after place and route. Multi-voltage designs require the appropriate power

Key Features and Benefits

- **Power Intent Consistency Checks:** Syntax and semantic checks on UPF that help validate the consistency of UPF prior to implementation. Incorrect power intent will result in incorrect low power design implementation. The UPF consistency checks ensure that the power intent specification driving low power implementation is syntactically and semantically correct
- **Architectural Checks:** Global checks at RTL for signals violating power architecture rules. VC LP validates the design in its entirety and checks the critical signal networks in the design for the various power modes. These checks help find connectivity s

Figure 4: VC LP's box-in-box schematic view

Conclusion

Adoption of advanced low power design techniques is growing rapidly to support ever-more sophisticated system level power management schemes. Fine-grained voltage control-based low power design techniques require stringent validation and checking throughout implementation and verification flows. VC LP's comprehensive and accurate low power static rule checks understand the most complex power intent and has the capacity and performance for the largest SoC designs. VC LP is in production deployment and adopted at industry-leading customers.

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