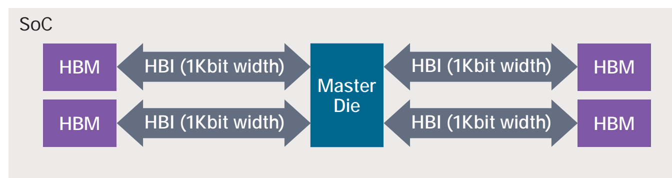
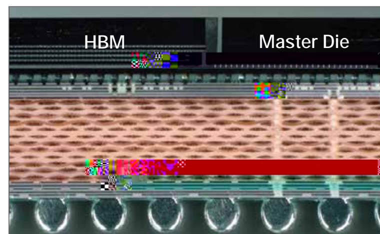
a cross-functional team to satisfy the design for test (DFT) requirements on a challenging multi-die system-on-chip (SoC) project with a master die chiplet and four High Bandwidth Memory (HBM) modules. We completed all DFT items and successfully shipped the product on schedule, at the target data rate, and without any impact on logic die size. ”

~Shinichiro Ikeda, Senior Principal Engineer, Socionext Inc.

Challenges

Project Overview

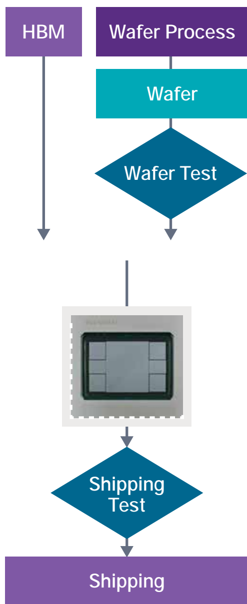




Silicon Interposer

Package Substrate (Organic)

BGA Balls


HBM
Wafer Process
Wafer
Wafer Test
Shipping Test
Shipping

		Test Flow	Test Item	WT	FT	DA
	(a)	Master Die Test	Master Die Test (including other IPs)			–
			Master die logic scan test (including PHY IP)			–
SLM SHS IP	(b)	HBM PHY IP Test	Analog parts test (PLL and DLL test)			–
			At speed loop back test			–
	(c)	HBI Connection Test and Repair	HBI connection test and lane repair between SoC and HBM	–		–
SLM SMS ext-RAM IP	(d)	HBM DRAM Test	HBM test via DFT circuit in SoC	–		–
	(e)	HBM DA Test	Fault analysis by HBM vendor via DA port	–	–