Overview

Synopsys SLM SHS IP is an automated hierarchical test solution for efficiently testing SoCs or designs using multiple IP/cores, including analog/mixed-signal IP, digital logic cores and interface IP. It significantly reduces test integration time by automatically creating a hierarchical IEEE 1500 network to access and control all IP/cores at the SoC level, and increases test quality of results (QoR), including optimizing test time and power through flexible test scheduling of IP and cores.

The solution also offers support for IEEE 1687 and enables standardized test and control access to complex interface IPs for efficient silicon debug and diagnostics, and allows silicon debug and diagnostics by enabling IP debug test modes from the SoC level. The system's highly automated design-for-test (DFT) implementation and hierarchical IP- and core-level test enables engineering teams to cut their test integration time to a matter of days and bring their designs

Hierarchical Architecture

Synopsys SLM SHS IP creates user-configurable and broadly adopted IEEE 1500 interfaces in the RTL for each IP/core and integrates the interfaces with a top-level control module or server while maintaining a standard interface at every level of design hierarchy.

IP Test Integr

Synopsys SLM SHS IP uses an IP/core view, which includes the I/O and test information, for creating IEEE 1500 interfaces, shown as wrappers in Figure 1. Synopsys SLM SHS IP can automatically create an IP view for any analog/mixed-signal IP, digital logic core or interface IP. To reduce the signal routes and congestion, SHS allows wrapped IP/cores to be integrated in a daisy-chain or ring configuration. Additionally, the system automatically creates verification testbenches, timing constraints and configuration files to enable faster design closure.

Re-Use IP Pa

Synopsys SLM SHS IP utilizes the IEEE 1500 network to port IP test patterns to the SoC level, eliminating the need to regenerate patterns and reducing test development time. The system automatically ports the serial access patterns to the SoC level.

Flexible Test

Synopsys SLM SHS IP provides flexibility to schedule individual IP and cores for parallel or serial testing to optimize test time and power consumption. The server manages hierarchical test access and control of the IP and can selectively enable IP to be tested in parallel. This flexible test scheduling capability can significantly reduce test time and test cost, especially for designs with limited I/Os.

eFUSE Progra

Synopsys SLM SHS IP helps improve SoC yield by enabling eFUSE programming through the server for calibration and trimming of analog/mixed-signal IP. The server collects the signature needed for calibration and trimming and programs it to the eFUSEs.

Tester Patterns

Synopsys SLM SHS IP creates tester-ready vectors in WIGL or STIL or 1687 based ICL/PDL or other common formats for the IP patterns ported to the SoC level and provides fault analysis and root-cause failure guidance based on silicon test results. SHS leverages IP debug test modes and enables diagnostics control and access from the SoC level. The system is compliant with the proposed IEEE 1687 standard, which allows re-use of SoC DFT instruments for board-level or system-level test and debug.

Silicon Bring-Up and D

Synopsys SLM SHS IP utilizes a test access port (TAP) to interactively communicate with the hierarchical IEEE 1500 network of the chip for post-silicon bring-up, system debug, diagnosis and characterization of IP. It enables post-silicon dignostics to be run from the engineer's desktop, without the need for expensive automatic test equipment.

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.