Meeting the Major Challenges of Modern Memory Design

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Overview

Memory lies at the heart of every electronics application, and demand is growing all the time. Users want ever greater capacity, throughput, and reliability. At the same time, time to market (TTM) goals and competitive pressures mandate that memories be developed in ever shorter shift left, digitization of memory design, and design for reliability.

Scaling Challenges

Unlike in the past, the design and development of new memories is not independent of process development. With today's deep submicron technologies, much closer cooperation between the design and process teams is necessary to provide the required improvements in memory density and performance. There are several factors and trends driving this evolution:

- The slowing of Moore's Law means that memory designers can no longer count on regular, predictable benefits from scaling alone
- The end of Dennard scaling has led to early design/architectural optimization, detailed optimization of physical layout design rules, and new process recipes
- The slowing of supply voltage scaling and the increasing effect of leakage currents have limited reductions in device power at new nodes
- Bitline and wordline parasitics have an increased effect in DRAM arrays
- The need for sufficiently high storage capacitor values drives higher aspect ratio capacitor structures and the use of materials with higher dielectric constants
- DRAM scaling has become more challenging due to cell capacitance, cell contact resistance, and row hammer effects
- Scaling of DRAM and NAND periphery is increasingly impacted by process variability, which reduces the design margin for the sensing circuits
- The number of layers in 3D NAND devices has grown to around 200 and is projected to increase to more than 500, driving innovation in high aspect ratio etching processes and process techniques to improve channel conductivity

All these effects have produced a technology-design gap that has resulted in suboptimal devices and process recipes, suboptimal memory performance, and late-stage design changes that increase TTM. Minimizing this gap requires co-optimization of materials, processes, and device structures with target designs to ensure directional correctness, and this need will grow even stronger with emerging memory technologies.

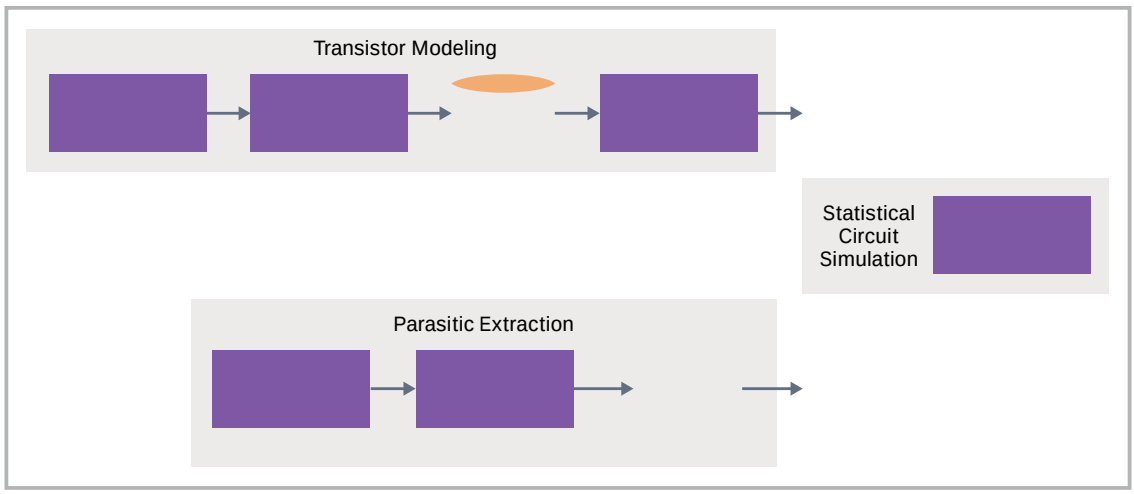
Design Technology Co-Optimization

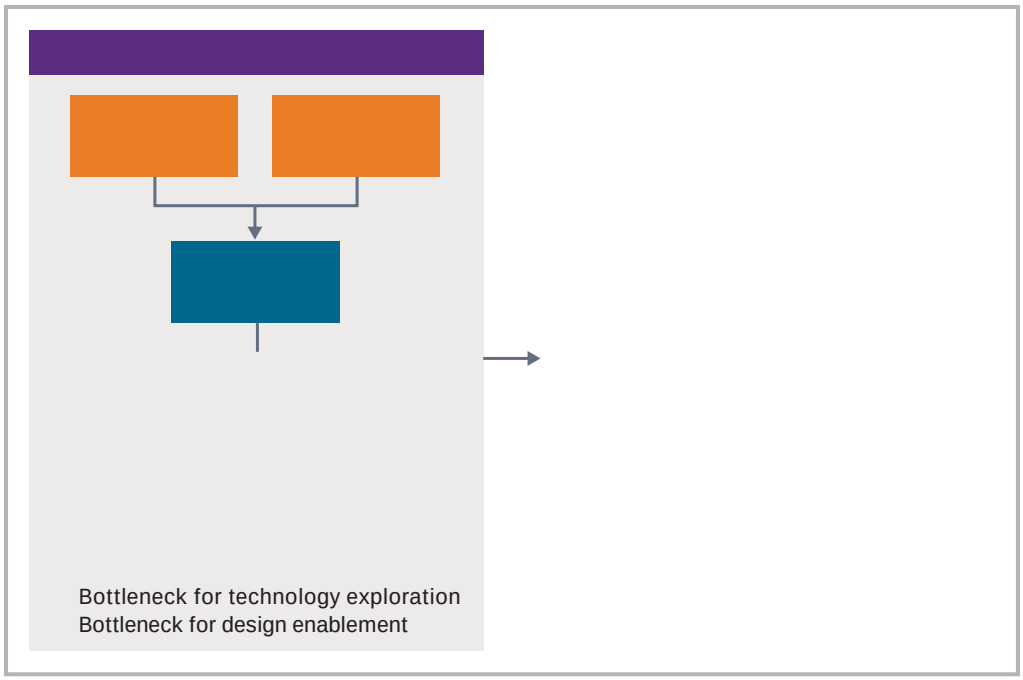
The collaboration between technology developers and designers required to address the scaling challenges is known as design technology co-optimization (DTCO). A memory DTCO flow must simulate the impact of technology choices and process variability on critical high precision analog circuits in the memory periphery, such as the sense amplifiers. This flow must include the following phases:

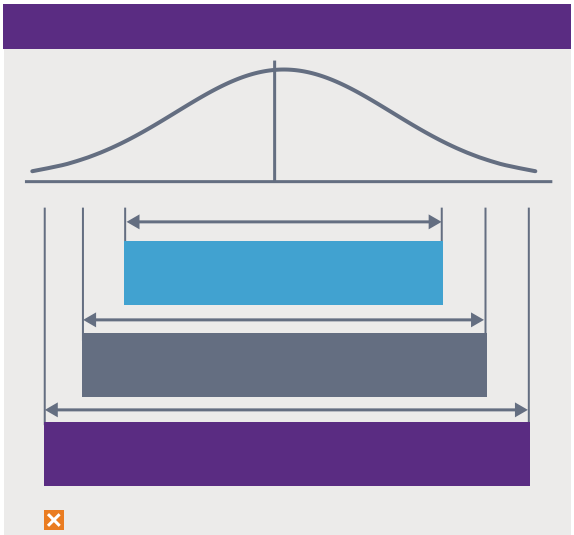
- Transistor modeling—technology computer-aided design (TCAD) simulates the fabrication process with its variability sources, followed by simulation of the transistor electrical characteristics and generation of data for subsequent extraction of a SPICE model
- Parasitic extraction—a 3D representation of the circuit is created, using as inputs a description of the interconnect process flow and a layout of the circuit element (for example a sense amplifier), and is fed to a parasitic field solver that extracts a circuit netlist and annotates it with RC parasitics
- SPICE simulation—the SPICE model and annotated netlist are simulated, to assess impact of variation on design metrics

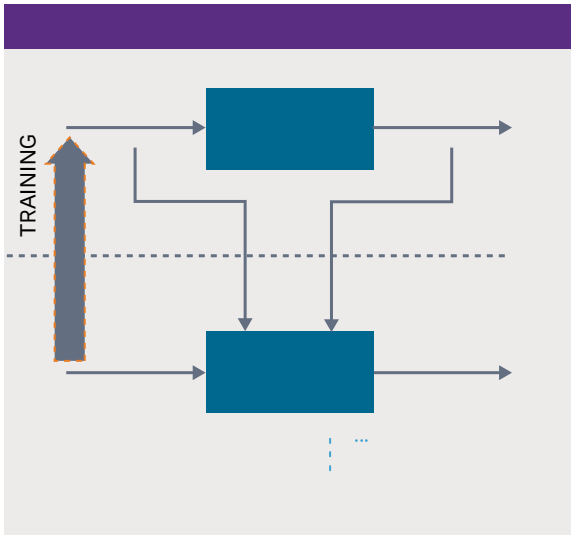
This flow develops a virtual process development kit (PDK) that enables early and rapid design exploration before wafers in the new process are available. The tight fusion of TCAD and SPICE technology provides design enablement with high-quality models that can be further refined when wafers are available and fabrication data can be gathered. The layout can be created early from virtual PDKs, with power, performance, and area (PPA) assessed from both pre-layout and post-layout netlists.

Synopsys provides a memory DTCO solution that meets all these requirements, and more. As shown in Figure 1, the heart of this flow is Synopsys PrimeSim™ SPICE, a high-performance simulator for analog, RF, and mixed-signal designs including memories. The transistor modeling phase uses Synopsys Sentaurus™ Process, which simulates the transistor fabrication steps, Synopsys Sentaurus Device, which simulates transistor performance, and Synopsys Mystic to extract SPICE models from the TCAD output. The SPICE netlist is generated by Synopsys Process Explorer process emulation and the Synopsys Raphael™ FX resistance and capacitance extraction tool.



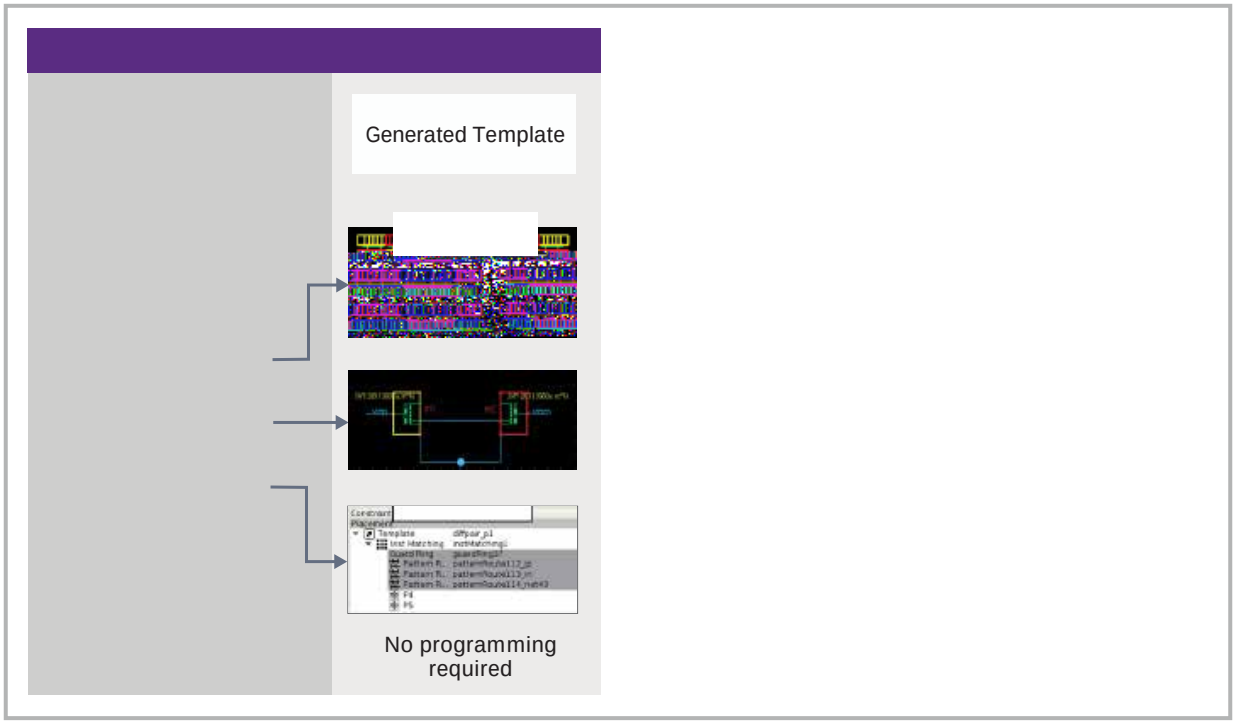

Bottleneck for technology exploration
Bottleneck for design enablement




TRAINING

To further shift left, there is opportunity to reduce the time and effort for the custom layout stage. The same sub-circuit topologies recur frequently in memory designs. As shown in Figure 5, the ability to reuse existing layouts created by expert designers is possible through the creation and application of templates that extract placement and routing patterns. Junior designers can create new layouts from those templates using whatever device size they need, saving time and leveraging the expert wisdom and experience embodied in the original layout.

Published case studies have shown that creating and using templates achieves more than 50% faster layout TAT for critical analog circuits in memories and produce more consistent layout quality regardless of the engineers' experience. The next frontier in layout design is the use of ML techniques to automate analog layout placement and routing, driving further improvements in layout productivity.



On the verification front, a digital-on-top flow enables efficient verification of memory datapaths using co-simulation and digital

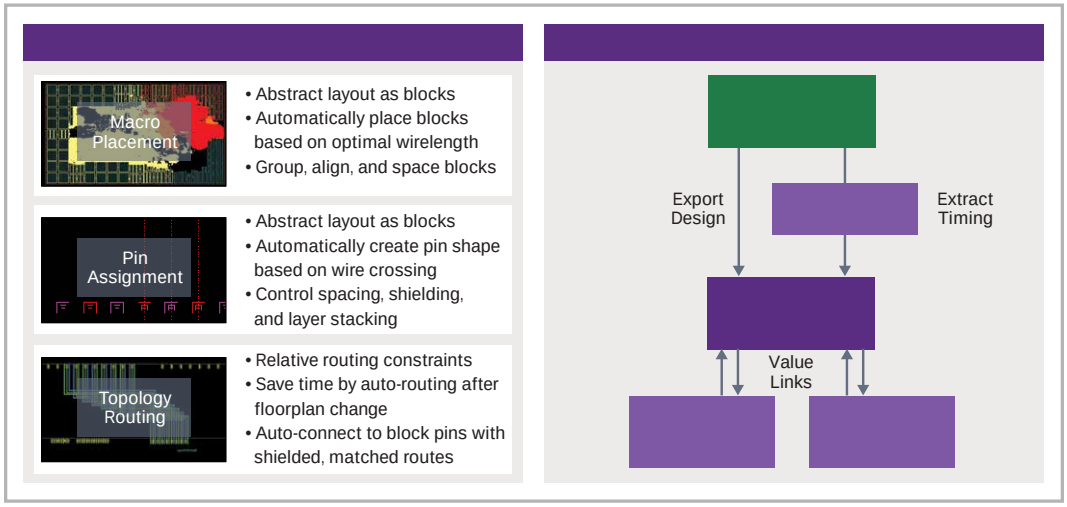


Figure 7: Synopsys digitization of memory development

For verification, Synopsys PrimeSim provides a unified workflow of next-generation simulation technologies, from gold-standard

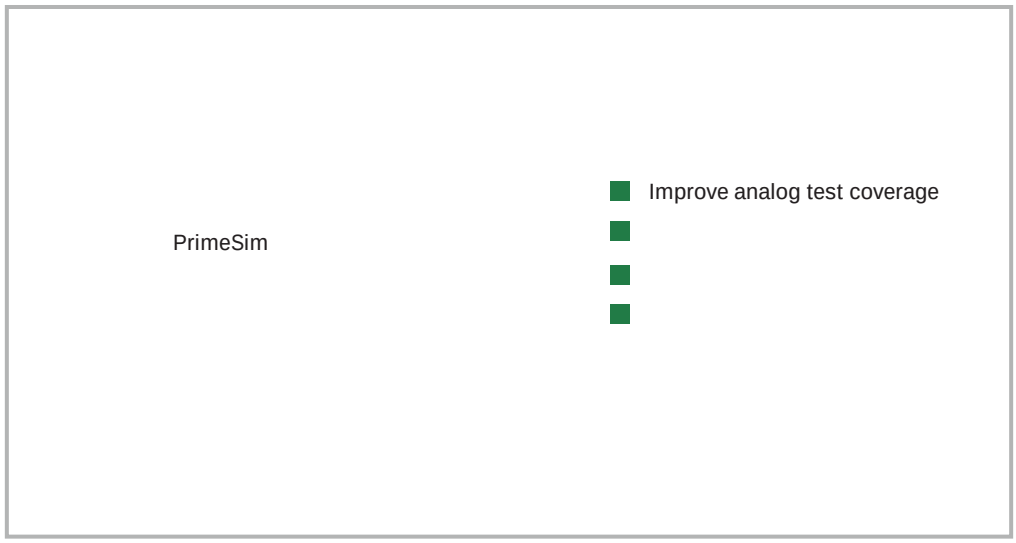
Both safety and reliability must span the entire silicon lifecycle, from design and verification through lab bring-up all the way to production use in the field. In the case of memory designs, the early and late stages of the lifecycle present the greatest challenges for reliability. Early chip failures (sometimes called infant mortality) shake out marginal devices, followed by a period (perhaps years) of low-risk operation. As silicon aging effects start to kick in, reliability goes down and failures become more common.

Ensuring Memory Safety and Reliability

To ensure reliability throughout the silicon lifecycle, the memory development process must include robust static and dynamic analysis to identify and mitigate potential failures across the silicon lifecycle before tapeout:

- Early life
  - – Static analog and digital circuit checks
  - – Analog fault simulation
- Normal life
  - – High-sigma Monte Carlo analysis
  - – Static power/signal net resistance checks
- End of life
  - – Dynamic electromigration/IR drop (EMIR) analysis
  - – Silicon aging analysis

An industry-leading solution meeting all these requirements is available with the comprehensive and flexible Synopsys PrimeWave Reliability Environment. It delivers a unified workflow around all the analysis technologies of Synopsys PrimeSim Reliability Analysis


PrimeSim
Improve analog test coverage

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